

ABSTRACT OF THE DISCLOSURE

The trace circuit comprises the event control circuit and two trace buffer memories. The event control circuit receives data on the control bus, address bus, and data bus and makes the data stored cyclically and alternately in the two buffer memories. Also, the event control circuit makes the two buffer memories output the store data cyclically and alternately.

Sub
a13

5

00000000 00000000 00000000 00000000